REMARKS

Claims 1-39 were examined. Claims 1-39 were rejected. Claims 1, 3, 12, 14, 21 and 31 are amended. Claims 30, 33-35 and 37-39 are cancelled. Applicants reserve the right to prosecute the former claims in a divisional or continuation application. Claims 1-29, 31-32 and 36 remain in the applications.

I. Claims Rejected Under 35 U.S.C. § 102

Claims 30-32 and 34-38 were rejected under 35 U.S.C. § 102(a) as being anticipated by Applicants' Admitted Prior Art (AAPA). Claims 30, 33-35 and 37-39 have been cancelled

II. Claims Rejected Under 35 U.S.C. § 103

A.

Claims 1, 3, 4, 6, 7, 10, and 11 were rejected under 35 U.S.C. §103(a) as being unpatentable over Applicants' Admitted Prior Art (AAPA) in view of U.S. Pat. Pub. No. 2001/0055840 to Verret ("Verret").

Claims 2 and 9 were rejected under 35 U.S.C. §103(a) as being unpatentable over AAPA in view of Verret in further view of Vogel.

Claim 5 was rejected under 35 U.S.C. §103(a) as being unpatentable over AAPA in view of Verret in further view of U.S. Pat. Pub. No. 2002/0074582 to Hiratani et al. ("Hiratani").

Claim 8 was rejected under 35 U.S.C. §103(a) as being unpatentable over AAPA in view of Verret in further view of U.S. Pat. No. 6,696,336 to DeBoer et al. ("DeBoer").

In order to establish a *prima facie* case of obviousness: (1) there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference; (2) there must be a reasonable expectation of success; and (3) the references when combined must teach or suggest all of the claim limitations. MPEP 2142. Applicant respectfully submits that a *prima facie* case of obviousness has not been established.

More particularly, the cited references in combination do not teach or suggest all of the claim limitations. Amended independent claim 1 includes the limitation of forming a first plug by depositing

a conductive layer on an entire surface of the resulting structure containing the first contact hole and planarizing the conductive layer, the first inter-layer insulation layer, and the etch stop layer at the same plane level of the conductive patterns. Thus, the conductive layer 27, the first inter-layer insulation layer 24 and the etch stop layer S are etched to the same plane as the conductive layer 27. See FIG. 2B. In contrast, Verret teaches that electrode 17 is not planar with respect to metal plug 47. FIG. 12. Thus, by examination of the structure, Verret does not teach the step of forming a first plug by depositing a conductive layer on an entire surface of the resulting structure containing the first contact hole and planarizing the conductive layer, the first inter-layer insulation layer, and the etch stop layer at the same plane level of the conductive patterns. Accordingly, because the references when combined do not teach of suggest all of the claim limitations, Applicants respectfully submit that independent claim 1 and its dependent claims are patentably allowable.

Moreover, none of the cited references in combination provide the suggestion or motivation to modify the references. The nature of the problem that Applicants' invention addresses is not the same as those in the references. MPEP 2143.1. Amended independent claim 1 includes the limitation of an attack barrier formed between the second plug and the conductive pattern. The purpose of the attack barrier is to protect layer 23B of etch stop layer S so that an electric short circuit between the gate electrode pattern G and a subsequently formed storage node contact plug 32 does not occur. See p.6, lns. 14-23. AAPA does not include such a limitation. In addition, although the integrated circuit in Verret includes a barrier layer 81, this barrier layer is used for an entirely different purpose. According to Verret, barrier layer 81 "serves as a diffusion barrier, for example, to keep unwanted materials out of the silicon layer 12, and also promotes adhesion between the layers above and below it." Col. 3, ¶ [0023]. In Applicants' invention, the attack barrier 51 is actually removed at a bottom part of the second contact hole 30 and, therefore, cannot serve as an adhesion material. See p.20, lns. 3-6. As such, there is no suggestion or motivation to modify the references to teach Applicants' invention. Accordingly, Applicants respectfully submit that independent claim 1 and its dependent claims are patentably allowable.

B.

Claims 12, 14, 15-16 and 19-20 were rejected under 35 U.S.C. §103(a) as being unpatentable over AAPA in view of Verret in further view of Hiratani.

Claims 13 and 18 were rejected under 35 U.S.C. §103(a) as being unpatentable over AAPA in view of Verret in further view of Vogel.

The cited references in combination do not teach or suggest all of the claim limitations. Amended independent claim 12 includes the limitations of (1) forming an etch stop layer having a multi-layer structure along a profile containing conductive patterns formed on a substrate and (2) forming an attack barrier on an entire surface of the resulting structure including the first plug. In contrast and as a preliminary matter, Hiratani does not teach an etch layer with a multi-layer structure. Moreover, Hiratani teaches a barrier on only a partial surface of the resulting structure. FIG. 3. Thus, by examination of the structure, Hiratani does not teach the step of forming an attack barrier on an entire surface of the resulting structure. Accordingly, in view of the arguments presented with respect to independent claims 1 and 12, the references when combined do not teach of suggest all of the claim limitations, and Applicants respectfully submit that independent claim 12 and its dependent claims are patentably allowable.

C.

Claims 21, 23-26, 28 and 29 were rejected under 35 U.S.C. §103(a) as being unpatentable over AAPA in view of Verret in further view of DeBoer.

The cited references in combination do not teach or suggest all of the claim limitations. Amended independent claim 21 includes the limitation of forming a first plug by depositing a conductive layer on an entire surface of the resulting structure containing the first contact hole and planarizing the conductive layer, the first inter-layer insulation layer, and the etch stop layer at the same plane level of the conductive patterns. Thus, the conductive layer 27, the first inter-layer insulation layer 24 and the etch stop layer S are etched to the same plane as the conductive layer 27. See FIG. 2B. In contrast, DeBoer teaches that transistor control gate 14A-B and 16A-C is not planar with respect to pad 18. FIG. 9. Thus, by examination of the structure, DeBoer does not teach the step of forming a first plug by depositing a conductive layer on an entire surface of the resulting structure containing the first contact hole and planarizing the conductive layer, the first inter-layer insulation layer, and the etch stop layer at the same plane level of the conductive patterns. Accordingly, in view of the arguments presented with respect to independent claims 1 and 21, the references when combined do not teach of suggest all of the claim limitations, and Applicants respectfully submit that independent claim 21 and its dependent claims are patentably allowable.

CONCLUSION

In view of the foregoing, Applicant believes that all claims now pending, namely claims 1-29, 31-32 and 36 patentably define the subject invention over the prior art of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: 3/6/06

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450 on 3-6-06

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